Amendments to the Claims

The listing of claims replaces all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1–8. (Cancelled)

Claim 9 (Currently amended). A mailbox apparatus for temporally storing messages, each message including a sequence of one or more data packets being transferred between a plurality of locations, the mailbox apparatus including a main memory, an ancillary memory, and a control unit which is arranged to:

receive a first message from one of the plurality of locations,

store at least a first data packet of the first message in the ancillary memory without storing the first data packet in the main memory and store ~~storing~~ at least one other data packet of the first message in the main memory, and

in response to a read signal, transmit the first data packet of the first message from the ancillary memory to another location, replenish the ancillary memory by transferring at least one of the at least one other data packet of the first message to the ancillary memory from the main memory and transmit the at least one of the at least one other data packet of the first message from the ancillary memory to another location; and

wherein the main memory is of a first type, and the second memory is of a second type that is different than the first type.

Claim 10 (previously presented). The mailbox apparatus according to claim 9 wherein the ancillary memory is a FIFO memory.

Claim 11 (previously presented). The mailbox apparatus according to claim 9 wherein the ancillary memory is implemented as registers.

Claim 12 (previously presented). The mailbox apparatus according to claim 9 wherein the control unit is further configured to transmit the stored data packet from the ancillary memory and replenish the ancillary memory on the same clock cycle.

Claim 13 (previously presented). The mailbox apparatus according to claim 9 wherein the ancillary memory is configured to store a number of data packets which is at least equal to a number of clock periods required to extract any data packet from the main memory.

Claim 14 (previously presented). The mailbox apparatus according to claim 9, further comprising a plurality of ancillary memories, each ancillary memory having a distinct corresponding location, each ancillary memory being arranged to store data packets to be transmitted to the corresponding location.

Claim 15 (previously presented). The mailbox apparatus according to claim 9, wherein the stored data packet comprises the first data packet and the at least one other stored data packet comprises a portion of the first message.

Claim 16 (Currently amended). A data processing system comprising:

a plurality of processors and a mailbox apparatus, a first processor of the plurality of processors being arranged to transfer a message to a second processor of the plurality of processors by transmitting the message as a series of data packets to the mailbox apparatus and sending a signal to the second processor to indicate the presence of the message in the mailbox apparatus, the second processor being arranged in response to send a read signal to the mailbox apparatus,

the mail box apparatus comprising a main memory of a first type, an ancillary memory of a second type that is different from the first type, and a control unit which is arranged to

receive the message from the first processor,

store at least a first data packet of the message in the ancillary memory without storing the first data packet in the main memory, and storing at least one other data packet of the message in the main memory, and

in response to the read signal, transmit the first data packet from the ancillary memory to another location, and replenish the ancillary memory by transferring at least one of the at least one other data packet of the message to the ancillary memory from the main memory.

Claim 17 (previously presented). The data processing system according to claim 16 wherein the ancillary memory is a FIFO memory.

Claim 18 (previously presented). The data processing system according to claim 16 wherein the ancillary memory is implemented as registers.

Claim 19 (previously presented). The data processing system according to claim 16 wherein the control unit is further configured to transmit the first data packet from the ancillary memory and replenish the ancillary memory on the same clock cycle.

Claim 20 (previously presented). The data processing system according to claim 16 wherein the ancillary memory is configured to store a number of data packets which is at least equal to a number of clock periods required to extract any data packet from the main memory.

Claim 21 (Currently amended). A method for temporally storing messages which include a sequence of one or more data packets and which are being transferred between a plurality of locations, the method including:

a) receiving a first message from one of the plurality of locations,

b) storing at least a first data packet of the first message in an ancillary memory without storing the first data packet in a ~~the~~ main memory, and storing one or more other data

packets of the first message in the ~~a~~ main memory, wherein the main memory is of a first type and the ancillary memory is of a second type that is different from the first type; and

c) in response to a read signal, transmitting the first data packet of the first message from the ancillary memory to another location, replenishing the ancillary memory by transferring at least one of the one or more other data packets of the first message to the ancillary memory from the main memory and transmit the at least one of the at least one other data packet of the first message from the ancillary memory to another location.

Claim 22 (previously presented). The method of claim 21 wherein step b) further comprises storing the first data packet in a FIFO memory.

Claim 23 (previously presented). The method of claim 21 wherein step b) further comprises storing the first data packet in one of a set of registers of the ancillary memory.

Claim 24 (previously presented). The method of claim 21 wherein step c) further comprises transmitting data from the ancillary memory to another location and replenishing the ancillary memory in the same clock cycle.

Claim 25 (previously presented). The method of claim 21 wherein step c) further comprises transferring the first data packet from the ancillary memory and replenishing the ancillary memory by transferring another data packet of the message from the main memory to the ancillary memory.

Claim 26 (Currently amended). A method for transferring a message between a first processor and a second processor using an apparatus having a main memory of a first type and an ancillary memory of a second type that is different from the first type, the method including:

a) transmitting the message from the first processor to the apparatus as a sequence of one or more data packets, and sending an interrupt signal to the second processor;

b) storing at least a first data packet of the message in the ancillary memory without storing the first data packet in the main memory, and storing at least one other data packet of the message in the main memory ,

c) in response to the interrupt signal, sending a read signal from the second processor to the apparatus,

d) in response to the read signal, transmitting the first data packet of the first message from the ancillary memory to second processor, replenishing the ancillary memory by transferring at least one of the at least one other data packet of the first message to the ancillary memory from the main memory and transmit the at least one of the at least one other data packet of the first message from the ancillary memory to another location.

Claim 27 (previously presented). The method of claim 26 wherein step c) further comprises transmitting the first data packet from the ancillary memory to the second processor, and replenishing the ancillary memory by transferring another data packet of the message from the main memory to the ancillary memory.

Claim 28 (previously presented). The method of claim 26 wherein step c) further comprises transmitting the first data packet from the ancillary memory to another location and replenishing the ancillary memory in the same clock cycle.